CLAIMS

We claim:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a dielectric gate stack formed on a channel region of the substrate, the dielectric gate stack having a top portion and a bottom portion;

the dielectric gate stack including an electron trapping layer of electron trapping material; and

a gate electrode connected with the top portion of the gate stack.

2. The semiconductor memory device of Claim 1 wherein the electron trapping material is selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

3. The semiconductor memory device of Claim 2 wherein the dielectric gate stack is comprised entirely of the electron trapping layer.

4. The semiconductor memory device of Claim 2 wherein the dielectric gate stack includes a first layer of dielectric material and a second layer of dielectric material configured such that the first layer of dielectric material is formed on the channel region of the substrate and the electron trapping layer is formed on the first layer of dielectric material and wherein the second layer of dielectric material is formed on the electron trapping layer.

5. The semiconductor memory device of Claim 4 wherein the first layer of dielectric material and the second layer of dielectric material are each comprised of silicon oxide.

6. A memory device as in Claim 4 wherein the first layer of dielectric material is formed of a different dielectric material than the second layer of dielectric material.

7. The semiconductor memory device of Claim 1 wherein the dielectric gate stack is comprised entirely of the electron trapping layer that comprises zirconium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Zr_xSi_yO_z$.

8. The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises aluminum oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Al_xSi_yO_z$.

9. The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises hafnium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Hf_xSi_yO_z$.

10. A semiconductor integrated circuit having the semiconductor memory devices of Claim 1 formed thereon.

11. A semiconductor memory device comprising:

a semiconductor substrate having a source and a drain separated by a channel region;

a first dielectric layer formed on the channel region of the substrate;

an electron trapping layer formed on the first dielectric layer;

a second dielectric layer formed on the electron trapping layer; and

a gate electrode connected with the second dielectric layer.

12. A method for forming a memory device comprising:

providing a semiconductor substrate;

forming a gate stack over a channel region of the substrate such that the gate stack includes a layer of electron trapping material; and

forming a gate electrode connected with a top portion of the gate stack.

13. The method for forming a memory device as in Claim 12, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

14. The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises forming a first layer of dielectric material over the channel region of the substrate and forming the layer of electron trapping material over the first layer of dielectric material and forming a gate electrode connected with the layer of electron trapping material.

15. The method for forming a memory device as in Claim 14, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

16. The method for forming a memory device as in Claim 15, wherein forming the first layer of dielectric material comprises formed the first layer of dielectric material with a silicon oxide material.

17. The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises:

forming a first layer of dielectric material over the channel region of the substrate;

forming the layer of electron trapping material over the first layer of dielectric material;

forming a second layer of dielectric material over the layer of electron trapping material; and

forming a gate electrode connected with a top portion of the second layer of dielectric material.

18. A method for forming a memory device as in Claim 17, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

19. The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with a silicon oxide material.

20. The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with different dielectric material.